[051] WHAT IS CLAIMED IS:

1. A buffer circuit in a mixed-voltage circuit operating in a power supply voltage, comprising:

a node;

a driver circuit coupled to the node comprising at least a first PMOS transistor having a substrate, a drain, a source, and a parasitic diode between the drain and the substrate, the driver circuit having an on-state and an off-state; and

a second PMOS transistor having a source and a drain, one of the source and drain of the second PMOS transistor being coupled to the substrate of the first PMOS transistor, wherein the second PMOS transistor is turned off when a first signal having a voltage level higher than the power supply voltage is provided on the node.

2. The circuit of claim 1, wherein a voltage at the substrate of the first PMOS transistor has a level substantially equal to that of the first signal when the first signal appears on the node.

3. The circuit of claim 1, wherein the second PMOS transistor has a gate and a substrate, the gate of the second PMOS transistor being coupled to the gate of the first PMOS transistor, the substrate of the second PMOS transistor being coupled to the substrate of the first PMOS transistor, and the other of the drain and source of the second PMOS transistor being connectable to receive the power supply voltage.

4. The circuit of claim 1, wherein the second PMOS transistor is turned on when the driver circuit operates in the on-state and a voltage at the node is approximately equal to the power supply voltage.

5. The circuit of claim 1, wherein the driver circuit further comprises two stacked NMOS transistors serially coupled to the first PMOS transistor, all of the first PMOS transistor and the two stacked NMOS transistors being off when the driver circuit is in the off state, and one of the first PMOS transistor or both of the two stacked NMOS transistors being on when the driver circuit is in the on state.

6. A buffer circuit operable in a power supply voltage coupled between a first circuit having a first power level and a second circuit having a second power level, comprising:

a node;

a driver circuit comprising a first transistor and a pair of stacked transistors, the first transistor having a gate, a source, and a drain, one of the source and the drain of the first transistor being coupled to the node, the stacked transistors comprising a second transistor and a third transistor;

a fourth transistor having a source and a drain, one of the source and drain of the fourth transistor being coupled to the gate of the first transistor, the other of the source and drain of the fourth transistor being coupled to the node, wherein the fourth transistor is turned on to provide a first bias to the gate of the first transistor

when a first signal having a voltage level higher than the power supply voltage appears at the node; and

a gate-tracking circuit coupled to the node and the second and third transistors.

7. The circuit of claim 6, wherein the gate-tracking circuit comprises a fifth transistor having a source, a drain, and a gate, one of the source and drain of the fifth transistor being coupled to the node, and the gate of the fifth transistor being coupled to both the second and third transistors.

8. The circuit of claim 6, wherein the fourth transistor has a substrate coupled to the substrate of the first transistor and a gate connectable to receive the power supply voltage.

9. The circuit of claim 7, wherein the fifth transistor is turned on when the first signal appears at the node.

10. The circuit of claim 6, wherein the first bias has a voltage level approximately equal to that of the first signal.

11. The circuit of claim 6, wherein the gate-tracking circuit further comprising a switch, wherein the switch is turned on when the buffer circuit is in a transmit mode.

12. The circuit of claim 11, wherein the switch includes a sixth transistor and a seventh transistor, each having a source, a drain, and a gate, one of the source and drain of the sixth transistor and one of the source and drain of the seventh transistor being coupled to the gate of the first transistor, the gate of the sixth transistor being connectable to receive the power supply voltage, and the gate of the seventh transistor being coupled to the other of the source and drain of the fifth transistor.

13. The circuit of claim 12, wherein the seventh transistor is turned on when a second signal having a voltage level lower than the power supply voltage appears at the node.

14. A buffer circuit connectable to receive a power supply voltage, comprising:

a node;

a driver circuit coupled to the node comprising at least a first PMOS transistor, the first PMOS transistor having a gate and a substrate, the driver circuit having an on-state and an off-state;

a second PMOS transistor having a source and a drain, one of the source and drain of the second PMOS transistor being coupled to the substrate of the first PMOS transistor, wherein the second PMOS transistor is turned off when a first signal having a voltage level higher than the power supply voltage appears at the node;

a first part of a tracking circuit coupled to the gate of the first PMOS transistor to provide a first bias to the gate of the first PMOS transistor when the first signal appears at the node; and

a second part of a tracking circuit coupled to the gate of the first PMOS transistor to provide a second bias to the gate of the first PMOS transistor when the driver circuit is in the off-state and a second signal having a voltage level no greater than the power supply voltage appears at the node.

15. The circuit of claim 14, wherein the driver circuit further comprises a pair of stacked NMOS transistors coupled to the first PMOS transistor.

16. The circuit of claim 14, wherein the voltage at the substrate of the first PMOS transistor is approximately equal to the voltage level of the first signal when the first signal appears at the node.

17. The circuit of claim 14, wherein the first bias has a voltage level approximately equal to the voltage level of the first signal.

18. The circuit of claim 14, wherein the second bias has a voltage level approximately equal to the power supply voltage.

19. The circuit of claim 14, wherein the first part comprises a third PMOS transistor having a gate, a source, a drain, and a substrate, the gate of the third

PMOS transistor is connectable to receive the power supply voltage, one of the source and drain of the third PMOS transistor is coupled to the node, the other of the source and drain of the third PMOS transistor is coupled to the gate of the first PMOS transistor, and the substrate of the third PMOS transistor is coupled to the substrate of the first PMOS transistor.

20. The circuit of claim 14, wherein the third PMOS transistor is turned on when the first signal appears at the node.

21. The circuit of claim 14, wherein the second part comprises a third PMOS transistor having a gate, a source, a drain, and a substrate, and the driver circuit comprises a first NMOS transistor and a second NMOS transistor, and wherein the gate of the third PMOS transistor is coupled to both the first and second NMOS transistors, one of the source and drain of the third PMOS transistor is coupled to the node.

22. The circuit of claim 21, wherein the third PMOS transistor is turned on when the first signal appears at the node.

23. The circuit of claim 21, wherein the second part further comprises a switch having a third NMOS transistor and a fourth PMOS transistor coupled in parallel, each of the third NMOS transistor and the fourth PMOS transistor having a gate, a source, and a drain, and wherein the gate of the third NMOS transistor is

connectable to receive the power supply voltage, the gate of the fourth PMOS transistor is coupled to both the substrate and the other of the source and drain of the third PMOS transistor, one of the source and drain of the third NMOS transistor is coupled to one of the source and drain of the fourth PMOS transistor, and the other of the source and drain of the third NMOS transistor is coupled to the other of the source and drain of the fourth PMOS transistor and further coupled to the gate of the first PMOS transistor.

24. The circuit of claim 23, wherein the fourth PMOS transistor is turned off when the first signal appears at the node.

25. A system having a plurality of components operating at different voltage levels, comprising:

a first chip including a first circuit;

a second chip including a second circuit;

a buffer circuit on the first chip having a receive mode and a transmit mode of operation and coupled between the first circuit and the second circuit, wherein the buffer circuit is connectable to a first power supply voltage and the second circuit is connectable to a second power supply voltage;

a node coupling the buffer circuit to the second circuit; and

a control signal terminal for providing a first control signal to switch the buffer circuit into the transmit mode, in which the buffer circuit receives at least one signal from the first circuit and outputs at least one signal to the second circuit, and for

providing a second control signal to switch the buffer circuit into the receive mode, in which the buffer circuit receives at least one signal from the second circuit and outputs at least one signal to the first circuit, wherein the buffer circuit comprises at least a driver circuit.

26. The system of claim 25, wherein the driver circuit comprises at least a first PMOS transistor having a drain and a substrate.

27. The system of claim 26, wherein the buffer circuit further comprises a second PMOS transistor having a source and a drain, one of the source and drain of the second PMOS transistor being coupled to the substrate of the first PMOS transistor, wherein the second PMOS transistor is turned off when a first signal having a voltage level higher than the power supply voltage appears at the node.

28. The system of claim 27, wherein the buffer circuit further comprises,

a first part of a tracking circuit coupled to the gate of the first PMOS transistor to provide a first bias to the gate of the first PMOS transistor when the first signal appears at the node, wherein the first bias has a voltage level approximately equal to the voltage level of the first signal, and

a second part of a tracking circuit coupled to the gate of the first PMOS transistor to provide a second bias to the gate of the first PMOS transistor when a second signal having a voltage level lower than the first power supply

voltage appears at the node, wherein the second bias has a voltage level approximately equal to the first power supply voltage in the receive mode.

29. The system of claim 25, wherein the first power supply voltage is lower than the second power supply voltage.

30. The system of claim 25, wherein the driver circuit is turned on in the transmit mode and turned off in the receive mode.

31. The system of claim 28, wherein the first part of the tracking circuit comprises a third PMOS transistor having a gate, a source, a drain, and a substrate, and wherein the gate of the third PMOS transistor is connectable to the first power supply voltage, one of the source and drain of the third PMOS transistor is coupled to the node, the other of the source and the drain of the third PMOS transistor is coupled to the gate of the first PMOS transistor, and the substrate of the third PMOS transistor is coupled to the substrate of the first PMOS transistor.

32. The system of claim 28, wherein the second part of the tracking circuit comprises a third PMOS transistor having a gate, a source, a drain, and a substrate, and the driver circuit of the buffer circuit comprises a first NMOS transistor and a second NMOS transistor, and wherein the gate of the third PMOS transistor is coupled to both the first and second NMOS transistors, one of the source and drain of the third PMOS transistor is coupled to the node.

33. The system of claim 32, wherein the second part of the tracking circuit further comprises a switch having a third NMOS transistor and a fourth PMOS transistor coupled to each other in parallel, each of the third NMOS transistor and the fourth PMOS transistor having a gate, a source, and a drain, and wherein the gate of the third NMOS transistor is connectable to the power supply voltage, the gate of the fourth PMOS transistor is coupled to both the substrate and the other of the source and drain of the third PMOS transistor, one of the source and drain of the third NMOS transistor is coupled to one of the source and drain of the fourth PMOS transistor, and the other of the source and drain of the third NMOS transistor is coupled to the other of the source and drain of the fourth PMOS transistor and further coupled to the gate of the first PMOS transistor.

34. The system of claim 25, wherein the buffer circuit further comprises an input circuit for receiving at least one signal from the second circuit and outputting at least one signal to the first circuit.

35. The system of claim 34, wherein the input circuit includes an inverter and a third PMOS transistor.

36. The system of claim 35, wherein the driver circuit of the buffer circuit further comprises a first NMOS transistor and a second NMOS transistor serially coupled to each other, and wherein the inverter has an input terminal coupled to

both the first and second NMOS transistors and a drain of the third PMOS transistor and an output terminal coupled to a gate of the third PMOS transistor, and the third PMOS transistor also has a source connectable to the first power supply voltage.